REMARKS

This is an amendment under 37 CFR §1.116. The purpose of this amendment is to put the claims in condition for allowance or, alternately, in better form for appeal. The amendments and specific remarks herein, to the extent they were not presented earlier, are now presented because they are necessitated by the reference citations and arguments made by the Examiner in the last office action. Since this amendment is being filed within two months of the mailing date of the final rejection, the courtesy of an advisory action is respectfully requested. Claims 2-21 are in this application. Claim 19 has been amended. Claim 1 has been cancelled. Claims 2-15 have been allowed.

The Examiner rejected claims 16-18 under 35 U.S.C. §102(b) as being anticipated by Barnes (U.S. Patent No. 6,369,632 B1). For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 16 recites:

> "a level shifting circuit having an input, an inverted output, and a non-inverted output, a logic high at the input having a first voltage, a logic high at the inverted output having a second voltage, a logic high at the non-inverted output having the second voltage, the second voltage being greater than the first voltage; and
>
> "a pull down circuit connected to the level shifting circuit that sinks current from the inverted output when the level shifting circuit sinks current from the inverted output, and from the non-inverted output when the level shifting circuit sinks current from the non-inverted output."

In rejecting the claims, the Examiner pointed to elements 42, 10, 11, 20, 21, 31, and 51-56 shown in FIG. 1 of Barnes as constituting the level shifting circuit required by claim 16. In addition, the Examiner pointed to input terminal 30 shown in FIG. 1 of Barnes as constituting the input required by claim 16, node 14 shown in FIG. 1 of Barnes as constituting the inverted output required by claim 16, and node

15 shown in FIG. 1 of Barnes as constituting the non-inverted output required by claim 16.

Further, the Examiner cited column 4, lines 63-65 (claim 7) of Barnes as teaching that a second voltage differs from a first voltage. The cited section of Barnes reads:

> "7. A circuit as claimed in claim 1 wherein a voltage supply to said input circuitry differs from a voltage supply to said output circuitry whereby said circuit output is level shifted."

Based on this, the Examiner argued that the second voltage (read by the Examiner to be the voltage on nodes 14 and 15) must be inherently greater than the first voltage (read by the Examiner to be the voltage on input terminal 30).

Applicant respectfully does not understand the Examiner's argument. The only positive voltage supply connected to the "input circuitry" is voltage supply 43 shown in FIG. 1 of Barnes. Thus, the phrase "a voltage supply to said input circuitry" recited by claim 7 of Barnes can only be read to be voltage supply 43. Similarly, the only positive voltage supply connected to the "output circuitry" is voltage supply 46 shown in FIG. 1 of Barnes. Thus, the phrase "a voltage supply to said output circuitry" recited by claim 7 of Barnes can only be read to be voltage supply 46.

Further, Barnes teaches in FIG. 1 that the level shifting is performed by a level shifting inverter (transistors 54 and 55). The level shifting inverter has inputs that receive a logic high voltage which is defined by voltage supply 43, and an output which has a logic high voltage that is defined by voltage supply 46. (See also from column 3, line 8, to column 4, line 10, of Barnes.)

Thus, although FIG. 1 of the Barnes reference teaches that level shifting takes place between input terminal 30 and output terminal 60, applicant can find no discussion in the Barnes reference that teaches or suggests that nodes 14 and 15

ever receive a logic high voltage that is greater than the logic high voltage received by input terminal 30.

Further, inherency requires that a condition always be present. However, from what can be determined, nodes 14 and 15 never receive a logic high voltage that is greater than the logic high voltage received by input terminal 30. Thus, since nodes 14 and 15 never receive a logic high voltage that is greater than the logic high voltage received by input terminal 30, nodes 14 and 15 can not inherently have a logic high voltage that is greater than the logic high voltage received by input terminal 30.

As a result, since Barnes does not teach or suggest that nodes 14 and 15 receive a logic high voltage that is greater than the logic high voltage received by input terminal 30, claim 16 is not anticipated by Barnes. In addition, since claims 17-18 depend either directly or indirectly from claim 16, claims 17-18 are not anticipated by Barnes for the same reasons as claim 16.

The Examiner objected to claims 19-21, but indicated that these claims would be allowable if amended to be in independent form to include all of the limitations of the base claim and any intervening claims. Claim 19 has been amended to be in independent form, and is believed to include all of the limitations of the base claim and any intervening claims. Claims 20-21 have not been amended as these claims depend from claim 19.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are requested.

Respectfully submitted,

Dated: 9-26-05 By: Mark C. Pickering

Mark C. Pickering
Registration No. 36,239
Attorney for Assignee

P.O. Box 300
Petaluma, CA 94953-0300
Telephone: (707) 762-5500
Facsimile: (707) 762-5504
Customer No. 33402